LISTING OF CLAIMS:

This listing of claims replaces all prior versions and listings of claims in this Application.

Claims 1-10 (Cancelled)

11. (New) A modulation and demodulation system, comprising:

a transmitter, comprising:

a serial-to-parallel converter that converts a received first bit-stream into a plurality of first sub bit-streams;

a plurality of Turbo Code encoders that correspond in number to the plurality of first sub bit-streams, wherein each Turbo Code encoder is coupled to a corresponding output of the serial-to-parallel converter;

a plurality of mappers that correspond in number to the plurality of Turbo Code encoders, wherein each mapper is coupled to an output of a corresponding Turbo Code encoder;

a channel selector that is coupled to each of the mappers for receiving an output from each of the corresponding mappers;

a complex inverse Fast Fourier Transform processor that is coupled to the channel selector for receiving the plurality of first sub-bit streams processed by the plurality of Turbo Code encoders, wherein the channel selector assigns the plurality of first sub-bit streams to a plurality of first sub-channels associated with the complex inverse Fast Fourier Transform processor, wherein the inverse Fast Fourier Transform processor outputs a plurality of first complex samples, and wherein the plurality of first complex samples each include an I sequence and a Q sequence; and

a receiver, comprising:

a complex Fast Fourier Transform processor that receives a plurality of second complex samples, wherein the plurality of second complex samples each include an I sequence and a Q sequence;

a channel deselector that receives an output from the complex Fast Fourier Transform processor and assigns the output from the complex Fast Fourier Transform processor to a plurality of second sub bit-streams;

a plurality of demappers that correspond in number to the plurality of second sub bit-streams, wherein each demapper is coupled to a corresponding output of the channel deselector;

a plurality of Turbo Code decoders that correspond in number to the plurality of demappers, wherein each Turbo Code decoder is coupled to a corresponding output of the plurality of demappers; and

a parallel-to-serial converter that converts a received plurality of second sub bit-streams into a second bit-stream.

12. (New) The modulation and demodulation system according to claim 11, wherein the transmitter further comprises:

a guard interval adder that receives the plurality of first complex samples from the inverse Fast Fourier Transform processor and adds a guard interval, wherein the plurality of first complex samples each include the I sequence and the Q sequence;

a symbol wave shaper that is coupled to the guard interval adder to filter the I sequence and the Q sequence of the plurality of first complex samples; and

an IQ modulator that is adapted to modulate the I sequence using a first carrier signal and the Q sequence using a second carrier signal to produce a transmitted signal.

13. (New) The modulation and demodulation system according to claim 12, wherein the receiver further comprises:

an IQ demodulator that is adapted to receive the transmitted signal and demodulate the I sequence using the first carrier signal and the Q sequence using the second carrier signal;

a guard interval remover that is coupled to the IQ demodulator for removing the guard interval, wherein the guard interval outputs the plurality of second complex samples, wherein the plurality of second complex samples each include an I sequence and a Q sequence;

a clock recovery circuit that provides clock synchronization to the IQ demodulator and the guard interval remover.

14. (New) The modulation and demodulation system according to claim 11, wherein the system is a universal mobile telecommunications system.

15. (New) The modulation and demodulation system according to claim 11, wherein the system is a baseband processing system.

16. (New) The modulation and demodulation system according to claim 11, wherein the system is capable of delivering data over at least one of wireless communication networks, wired communication networks and satellite internet protocol networks.

17. (New) The modulation and demodulation system according to claim 11, wherein the system is capable of delivering at least one of multimedia data, voice data, voice over internet protocol data.

18. (New) The modulation and demodulation system according to claim 16, wherein the system is capable of delivering at least one of high-speed broadband information and multimedia entertainment services.

19. (New) The modulation and demodulation system according to claim 11, wherein the inverse Fast Fourier Transform processor is adapted to implement an orthogonal frequency division technique.

20. (New) The modulation and demodulation system according to claim 11, wherein the Fast Fourier Transform processor is adapted to implement an orthogonal frequency division technique.

21. (New) The modulation and demodulation system according to claim 11, wherein each of the plurality of Turbo code encoders has a coding rate of 1/3 and a constraint length of k=4.

22. (New) The modulation and demodulation system according to claim 11, wherein each of the plurality of Turbo code decoders has a coding rate of 1/3 and a constraint length of k=4.

23. (New) The modulation and demodulation system according to claim 11, wherein each of the plurality of Turbo code decoders uses a soft-input soft-output 8-state Log-MAP decoder.

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24. (New) The modulation and demodulation system according to claim 11, wherein each of the plurality of demappers is an 8-Phase Shift Keying demapper that produces a soft-decision value output.

25. (New) The modulation and demodulation system according to claim 11, wherein the serial-to-parallel converter is an M-bit serial-to-parallel converter that subdivides the received first bit-stream having R-Mbps into multiple slow-speed S-Mbps first sub-bit streams, where S-Mbps is equal to R-Mbps divided by a number of the first sub-channels associated with the inverse Fast Fourier Transform processor.

26. (New) The modulation and demodulation system according to claim 11, wherein the inverse Fast Fourier Transform processor is an N-point inverse Fast Fourier Transform processor and wherein multiple adjacent first sub-channels transmit their carrier frequency orthogonal to each other.

27. (New) The modulation and demodulation system according to claim 11, wherein the Fast Fourier Transform processor is an N-point Fast Fourier Transform processor and wherein multiple adjacent second sub-channels transmit their carrier frequency orthogonal to each other.

28. (New) The modulation and demodulation system according to claim 11, wherein the channel selector controls channel hopping by reassigning a selected one of the plurality of first sub bit-streams to a different one of the plurality of first sub-channels.

29. (New) The modulation and demodulation system according to claim 11, wherein the first bit-stream is received from a Media Access Layer.

30. (New) The modulation and demodulation system according to claim 11, wherein the second bit-stream is transmitted to a Media Access Layer.

31. (New) The modulation and demodulation system according to claim 11, wherein the first carrier signal is a Sine wave.

32. (New) The modulation and demodulation system according to claim 11, wherein the second carrier signal is a Cosine wave.

33. (New) A modulation system having a transmitter comprising:

a serial-to-parallel converter that converts a received bit-stream into a plurality of sub bit-streams;

a plurality of Turbo Code encoders that correspond in number to the plurality of sub bit-streams, wherein each Turbo Code encoder is coupled to a corresponding output of the serial-to-parallel converter;

a plurality of mappers that correspond in number to the plurality of Turbo Code encoders, wherein each mapper is coupled to an output of a corresponding Turbo Code encoder;

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a channel selector that is coupled to each of the mappers for receiving an output from each of the corresponding mappers; and

a complex inverse Fast Fourier Transform processor that is coupled to the channel selector for receiving the plurality of sub-bit streams processed by the plurality of Turbo Code encoders, wherein the channel selector assigns the plurality of sub-bit streams to a plurality of sub-channels associated with the complex inverse Fast Fourier Transform processor, wherein the inverse Fast Fourier Transform processor outputs a plurality of complex samples, and wherein the plurality of complex samples each include an I sequence and a Q sequence.

34. (New) A demodulation system having a receiver comprising:

a complex Fast Fourier Transform processor that receives a plurality of complex samples, wherein the plurality of complex samples each include an I sequence and a Q sequence;

a channel deselector that receives an output from the complex Fast Fourier Transform processor and assigns the output from the complex Fast Fourier Transform processor to a plurality of sub bit-streams;

a plurality of demappers that correspond in number to the plurality of sub bit-streams, wherein each demapper is coupled to a corresponding output of the channel deselector;

a plurality of Turbo Code decoders that correspond in number to the plurality of demappers, wherein each Turbo Code decoder is coupled to a corresponding output of the plurality of demappers and process the corresponding output from the complex Fast Fourier Transform processor; and

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a parallel-to-serial converter that converts a received plurality of sub bit-streams into a bit-stream.

35. (New) A method of transmitting high speed digital data comprising:

receiving serial data at a rate of R-Mbps;

sub-dividing the serial data into M sub bit-streams;

encoding each of the M sub bit-streams independently;

mapping the encoded sub bit-streams into constellation points to select values of an I component and a Q component;

mapping the I component into a real part and the Q component into an imaginary part; and

performing a complex N-point inverse Fast Fourier Transform for data associated with each of the independently encoded M sub bit-streams to produce an I sequence and a Q sequence of N samples.

36. (New) The method of transmitting high speed digital data according to claim 35, further comprising:

adding a guard interval to the I sequence and the Q sequence of N samples;

filtering the I sequence and the Q sequence of N samples;

modulating the I sequence using a first carrier signal;

modulating the Q sequence using a second carrier signal; and

summing the modulated I sequence and the modulated Q sequence to produce a transmitted signal.

37. (New) The method of transmitting high speed digital data according to claim 35, wherein the step of encoding each of the M sub bit-streams independently includes encoding with a coding rate of 1/3 and a constraint length of k=4 to generate a 3-bit symbol having one data bit and two parity bits.

38. (New) The method of transmitting high speed digital data according to claim 37, wherein the step of mapping the encoded sub bit-streams into constellation points to select values of an I component and a Q component includes mapping the 3-bit symbol into 8-phase shift keying constellation points.

39. (New) The method of transmitting high speed digital data according to claim 36, wherein the first carrier signal is a sine wave.

40. (New) The method of transmitting high speed digital data according to claim 36, wherein the second carrier signal is a cosine wave.

41. (New) The method of transmitting high speed digital data according to claim 35, wherein the serial data at is received from a Media Access Layer.

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42. (New) A method of receiving high speed digital data comprising:

performing a complex N-point Fast Fourier Transform on an I sequence and a Q sequence of N samples to produce N complex point data;

deselecting each of the N complex points data for each set of the I sequence and the Q sequence of N samples associated with each of the M sub bit-streams;

demapping each of the N complex point data for each of the M sub bit-streams to produce soft decision values;

iteratively decoding the soft decision values to produce a final hard-decoded bit for each of the M sub bit-streams; and

serially transmitting each of the final hard-decoded bit for each of the M sub bit-streams at a rate of R-Mbps.

43. (New) The method of transmitting high speed digital data according to claim 42, further comprising:

demodulating the I sequence using a first carrier signal;

demodulating the Q sequence using a second carrier signal; and

removing a guard interval from the I sequence and the Q sequence of N samples.

44. (New) The method of transmitting high speed digital data according to claim 42, wherein the step of iteratively decoding the soft decision values includes decoding with a coding rate of 1/3 and a constraint length of k=4.

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45. (New) The method of transmitting high speed digital data according to claim 42, wherein the step of demapping each of the N complex point data for each of the M sub bit-streams to produce soft decision values includes demapping into 8-phase shift keying constellation points.

46. (New) The method of transmitting high speed digital data according to claim 43, wherein the first carrier signal is a sine wave.

47. (New) The method of transmitting high speed digital data according to claim 43, wherein the second carrier signal is a cosine wave.

48. (New) The method of transmitting high speed digital data according to claim 42, wherein the data is serially transmitted to a Media Access Layer.